

178. (new) A memory element, comprising:

a first dielectric layer;

a conductive layer formed over said first dielectric layer;

a second dielectric layer formed over said conductive layer;

a programmable resistance material in electrically communication with said conductive layer, substantially all of said communication occurring through at least one edge of said conductive layer.

179. (new) The memory element of claim 178, wherein said first dielectric layer has a sidewall surface, said conductive layer being formed over said sidewall surface.

180. (new) The memory element of claim 179, wherein said edge is a top edge of said conductive layer.

181. (new) The memory element of claim 179, wherein said conductive layer includes a sidewall layer.

182. (new) The memory element of claim 179, wherein said conductive layer is a conductive sidewall spacer.

183. (new) The memory element of claim 179, wherein said conductive layer is a conductive liner.

184. (new) The memory element of claim 179, wherein said conductive layer is cup-shaped, said edge being a rim of said cup-shaped layer.

185. (new) The memory element of claim 179, wherein said conductive layer is formed over a sidewall surface of an opening in said first dielectric layer, the sidewall surface of said first dielectric layer corresponding to the sidewall surface of said opening.

186. (new) The memory element of claim 179, wherein said conductive layer is formed over substantially all of the bottom surface of said opening.

187. (new) The memory element of claim 185, wherein said opening is a trench or a hole.

188. (new) The memory element of claim 185, wherein said opening passes through said first dielectric layer and exposes an underlying substrate.

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189. (new) The memory element of claim 178, wherein said conductive layer is substantially horizontally disposed.

190. (new) The memory element of claim 178, wherein said edge is adjacent to a sidewall surface of said programmable resistance material.

191. (new) The memory element of claim 178, wherein said edge at least partially circumscribes said programmable resistance material.

192. (new) The memory element of claim 178, wherein said programmable resistance material and said conductive layer having an area of contact that forms a band at least

partially about a lateral periphery of said programmable resistance material.

193. (new) The memory element of claim 178, wherein said edge has a dimension in at least one direction which is between 50 and 1000 Angstroms.

194. (new) The memory element of claim 178, wherein the area of contact between said programmable resistance material and said conductive layer is at least a portion of an annulus.

C1 195. (new) The memory element of claim 178, wherein said conductive layer comprises at least one material selected from the group consisting of titanium nitride, titanium aluminum nitride, titanium carbonitride, titanium silicon nitride, carbon, N- doped polysilicon, titanium tungsten, tungsten silicide, tungsten, molybdenum, N+ doped polysilicon.

196. (new) The memory element of claim 178, wherein said programmable resistance material includes a phase change material.

197. (new) The memory element of claim 178, wherein said programmable resistance material includes a chalcogen element.

198. (new) The memory element of claim 178, wherein said edge includes one or more protruding portions extending to terminal ends adjacent said programmable resistance material.

199. (new) The memory element of claim 178, wherein substantially all communication between said conductive layer and said programmable resistance material occurs through at least one of said protruding portions.

200. (new) The memory element of claim 178, wherein said electrical communication occurs through a portion of said edge.

201. (new) The memory element of claim 178, wherein said first and said second dielectric layers are formed of the same dielectric material.

C 202. (new) A memory element, comprising:

a first dielectric layer;

an electrical contact formed over said first dielectric layer;

a second dielectric layer formed over said electrical contact, at least a portion of said electrical contact being sandwiched between said first and second dielectrics, said electrical contact having an exposed surface between said first and said second dielectric layers; and

a programmable resistance material electrically coupled to said exposed surface.

203. (new) The memory element of claim 202, wherein first dielectric layer has a sidewall surface, said electrical contact formed over said sidewall surface.

204. (new) The memory element of claim 203, wherein said exposed surface is a top surface of said electrical contact.

205. (new) The memory element of claim 203, wherein said electrical contact includes a sidewall layer formed over said sidewall surface, said exposed surface being a being a top surface of said sidewall layer.

206. (new) The memory element of claim 203, wherein said electrical contact is a conductive sidewall spacer.

207. (new) The memory element of claim 203, wherein said electrical contact is a conductive liner.

208. (new) The memory element of claim 203, wherein said electrical contact is cup-shaped, said top surface being a rim of said cup-shaped electrical contact.

209. (new) The memory element of claim 203, wherein said electrical contact is formed over a sidewall surface of an opening in said first dielectric layer, said sidewall surface of said opening corresponding to the sidewall surface of said dielectric.

210. (new) The memory element of claim 209, wherein said electrical contact is formed over substantially all of the bottom surface of said opening.

211. (new) The memory element of claim 209, wherein said opening is a trench or a hole.

212. (new) The memory element of claim 209, wherein said opening passes through said first dielectric layer and exposes an underlying substrate.

213. (new) The memory element of claim 202, wherein said electrical contact includes a substantially horizontally disposed conductive layer.

214. (new) The memory element of claim 202, wherein said exposed surface is electrically coupled to a sidewall surface of said programmable resistance material.

C1 215. (new) The memory element of claim 202, wherein said exposed surface at least partially circumscribes said programmable resistance material.

216. (new) The memory element of claim 202, wherein said programmable resistance material and said electrical contact have an area of contact that forms a band at least partially about a lateral periphery of said programmable resistance material.

217. (new) The memory element of claim 202, wherein said electrical contact has a thickness between 50 and 1000 Angstroms at the area of contact with said programmable resistance material.

218. (new) The memory element of claim 202, wherein the area of contact between said programmable resistance material and said electrical contact is at least a portion of an annulus.

219. (new) The memory element of claim 202, wherein said electrical contact comprises at least one material selected from the group consisting of titanium nitride, titanium aluminum nitride, titanium carbonitride, titanium silicon nitride, carbon, N- doped polysilicon, titanium tungsten, tungsten silicide, tungsten, molybdenum, N+ doped polysilicon.

220. (new) The memory element of claim 202, wherein said programmable resistance material includes a phase change material.

221. (new) The memory element of claim 202, wherein said programmable resistance material includes a chalcogen element.

222. (new) The memory element of claim 202, wherein said exposed surface includes one or more protruding portions extending to terminal ends adjacent said programmable resistance material.

223. (new) The memory element of claim 202, wherein substantially all communication between said electrical contact and said programmable resistance material occurs through at least one of said protruding portions.

224. (new) The memory element of claim 206, wherein said conductive sidewall spacer comprises a first sidewall layer formed over said first dielectric and a second sidewall layer formed over a sidewall surface of said first sidewall layer.

225. (new) The memory element of claim 224, wherein the resistivity of said first sidewall layer is less than the resistivity of said second sidewall layer, said programmable resistance material is electrically coupled with a top surface of said second sidewall layer.

226. (new) The memory element of claim 224, wherein said first layer comprises at least one material selected from the group consisting of titanium tungsten, tungsten silicide, tungsten, molybdenum, N+ doped polysilicon and titanium nitride.

227. (new) The memory element of claim 224, wherein said second layer comprises at least one material selected from the group consisting of titanium nitride, titanium carbonitride, titanium aluminum nitride, titanium silicon nitride, carbon, and N- doped polysilicon.

228. (new) The memory element of claim 202, wherein said programmable resistance material is a phase-change material.

229. (new) The memory element of claim 202, wherein said programmable resistance material includes a chalcogen element.

230. (new) The memory element of claim 202, wherein said first and second dielectric layers are formed of the same dielectric material.

231. (new) A memory element, comprising:

a conductive sidewall spacer formed over a sidewall surface of a dielectric layer;

a programmable resistance material in electrical communication with said conductive sidewall spacer.

232. (new) The memory element of claim 231, wherein said programmable resistance material is electrically coupled to a top surface of said conductive spacer.

233. (new) The memory element of claim 231, wherein said top surface includes one or more protruding portions extending to a terminal end adjacent said programmable resistance material.

234. (new) The memory element of claim 233, wherein substantially all electrical communication occurs through at least one of said protrusions.

235. (new) The memory element of claim 233, wherein substantially all electrical communication occurs through one or more of said terminal ends.

236. (new) The memory element of claim 231, wherein said conductive sidewall spacer comprises at least one material selected from the group consisting of titanium nitride, titanium aluminum nitride, titanium carbonitride, titanium silicon nitride, carbon, N-doped polysilicon, titanium

tungsten, tungsten silicide, tungsten, molydenum, N+ doped polysilicon.

237. (new) The memory element of claim 231, wherein said conductive sidewall spacer comprises a first sidewall layer formed on said first dielectric and a second sidewall layer formed on a sidewall surface of said first sidewall layer.

238. (new) The memory element of claim 237, wherein the resistivity of said first sidewall layer is less than the resistivity of said second sidewall layer.

239. (new) The memory element of claim 237, wherein said first layer comprises at least one material selected from the group consisting of titanium tungsten, tungsten silicide, tungsten, molydenum, N+ doped polysilicon and titanium nitride.

240. (new) The memory element of claim 237, wherein said second layer comprises at least one material selected from the group consisting of titanium nitride, titanium carbonitride, titanium aluminum nitride, titanium silicon nitride, carbon, and N- doped polysilicon.

241. (new) The memory element of claim 238, wherein said programmable resistance material is electrically coupled to a top surface of said second sidewall layer.

242. (new) The memory element of claim 231, wherein said conductive spacer is formed over a sidewall surface of an opening in said dielectric layer, the sidewall surface of

said opening corresponding to the sidewall surface of said dielectric.

243. (new) The memory element of claim 231, wherein said opening is a trench.

244. (new) The memory element of claim 231, wherein said opening is a hole.

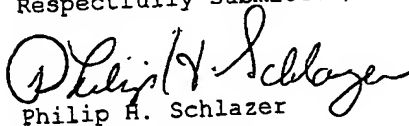
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245. (new) The memory element of claim 242, wherein said opening passes through said dielectric layer so as to expose an underlying substrate.

246. (new) The memory element of claim 231, wherein said programmable resistance material comprises a phase-change material.

SUMMARY

Claims 84-177 have been cancelled. Claims 178-246 have been added. Applicant respectfully requests reconsideration, withdrawal of the outstanding rejections, and notifications of allowance. Should the Examiner have any questions or suggestions regarding the prosecution of this application, he is asked to contact applicant's representative at the telephone number listed below.

Respectfully submitted,


Philip H. Schlazer
Reg. No. 42,127

Date: 7 January 2003
Energy Conversion Devices
2956 Waterview
Rochester Hills, MI 48309

Phone (248) 293-0440 extension 6260
Fax (248) 844-2273